CORNERSTONE

Design guidelines for the second fabrication call – May 2017

Mask submission deadline – Friday 30th June 2017

1. File format

Designs must be submitted in a Graphical Database System file format (extension .gdsII). Ensure a manufacturing grid size of no smaller than 1 nm is used.

We recommend dedicated lithography editing software is used in the design of the .gdsII file.

2. Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing. For this second call, we will process chips with a 220 nm thick silicon core on a 3 µm thick BOX (Buried OXide) layer. We will offer two etch processes: 1) a shallow silicon etching of 70 nm, and 2) a deep silicon etching of 220 nm to the BOX layer. In addition, we will offer metal heaters on top of a 1 µm thick silicon dioxide cladding layer.

2.1 Design area

The standard user cell has dimensions of **7 x 7 mm^2**. If cleaved facets are required for edge coupling, the total writing area should be reduced to 7 x 6 mm^2 as an overlay (or bleed) of 500 µm should be included, as shown in Figure 1. Please note that the input/output waveguides should extend into the bleed area.

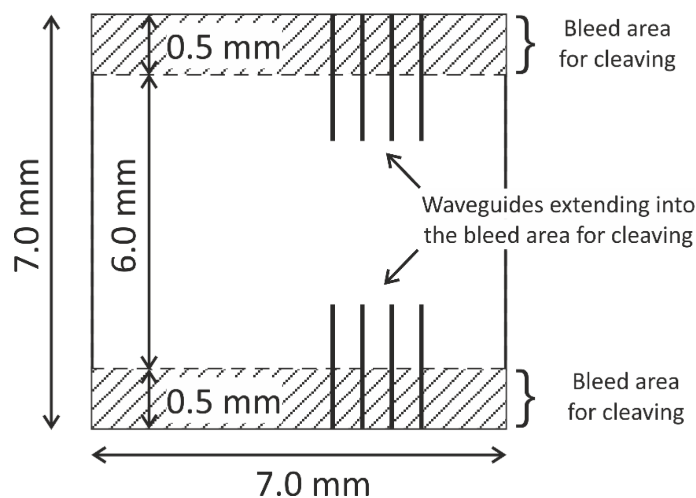

Figure 1 – User cell design area layout.

2.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers) – GDS Layer 6 (Dark field) – 70 nm

This layer is used to define grating couplers, which are fabricated with 70 nm shallow silicon etching. Positive tone e-beam resist is used, therefore the drawn area is etched.

Silicon Etch 2 (Waveguiding layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – 220 nm

This layer defines the waveguides, and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following etching to the BOX. During fracturing processing for the e-beam, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

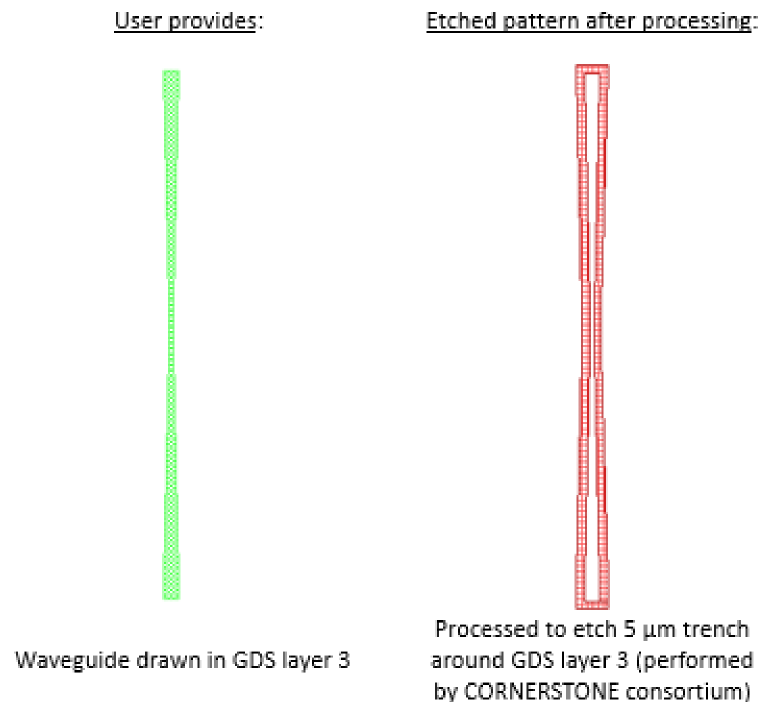

Figure 2 - Description of GDS layer 3 processing.

GDS Layer 4: Drawn objects on this layer will be exposed to the silicon etch to the BOX. This layer is intended for photonic crystal, and similar structures that require small feature sizes (150 nm < feature size < 300 nm). This layer will be written with an E-beam spot size of approximately 5 nm to ensure accurate translation of patterns into the resist. Therefore, the pattern density for this layer should be less than 0.5% of the total design area in order to reduce the E-beam writing time. An example photonic crystal structure is shown in Figure 3. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by the CORNERSTONE consortium there is a continuous waveguide.

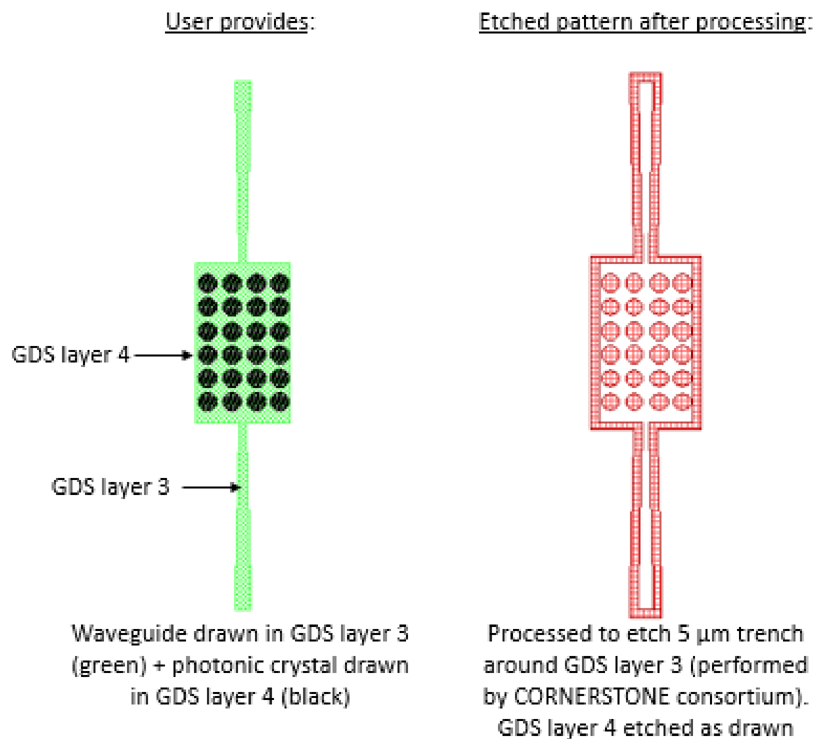

Figure 3 – Example photonic crystal structure using GDS layers 3 & 4.

Metal Layer 1 – GDS Layer 39 (Light field)

This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 900 nm for the best compromise between power efficiency and tunability.

Metal Layer 2 – GDS Layer 13 (Light field)

This layer defines the heater contact pads and labels. Drawn objects on this layer will remain after metal lift-off.

A silica (HSQ) cladding, conforming to Metal Layer 1 (GDS layer 39), will be added following the lift-off of all metals. This will protect the filament and increase its longevity.

An example heater layout for a straight waveguide is included in the GDSII template file. The contact pads can be modified according to your probe design.

Cell Outline – GDS Layer 99

This layer defines the design space (7 x 7 mm^2).

Bleed Area – GDS Layer 98

This layer defines the bleed area that will be cleaved if requested by the user. Ensure that waveguides extend fully into this area.

If no cleaving is required, users can fill the entire design space defined in GDS layer 99.

Note: You do not need to add fabrication alignment marks to your design.

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2.3 Minimum feature sizes and tolerances

Minimum feature sizes for each GDS layer are detailed in Table 1.

A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

An overlap of at least 100 nm between GDS layer 6 (Silicon Etch 1 – 70 nm) and GDS layers 3 & 4 (Silicon Etch 2 – 220 nm) is recommended to account for the alignment tolerance between layers.

An overlap of at least 50 µm between GDS layer 39 (Metal Layer 1) and GDS layer 13 (Metal Layer 2) is recommended for optimal heater performance.

2.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number/s	Field	Maximum pattern density	Minimum feature size
Silicon Etch 1 (70 nm)	6	Dark	N/a	150 nm
Silicon Etch 2 (220 nm)	3	Light	N/a	150 nm
	4	Dark	0.5%	
Metal Layer 1	39	Light	N/a	600 nm
Metal Layer 2	13	Light	N/a	2 µm
Cell Outline	99	N/a	N/a	N/a
Bleed Area	98	N/a	N/a	N/a

2.5 GDSII template file

A GDSII template file titled 'CORNERSTONE MPW Run 2 GDSII Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

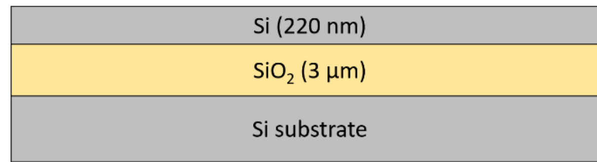
3. Process flow

The patterns will be processed by e-beam lithography on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

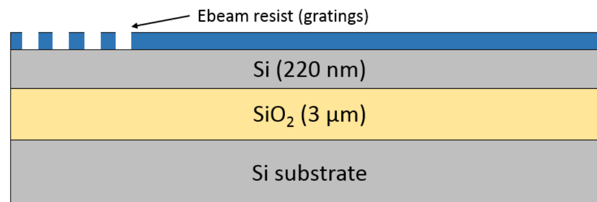
- Crystalline silicon (Si) substrate with a thickness h_{sub} = 675 ± 15 µm
- Thermal silica (SiO_2) BOX layer with a thickness h_{box} = 3 µm
- Crystalline silicon (Si) core layer with a thickness h_{wg} = 220 nm

The schematic description of the process flow is given below:

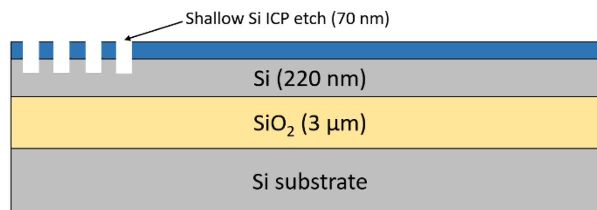
1. Starting SOI substrate



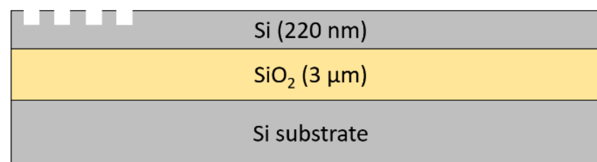
2. E-beam patterning for Silicon Etch 1 (GDS layer 6) – 70 nm etch



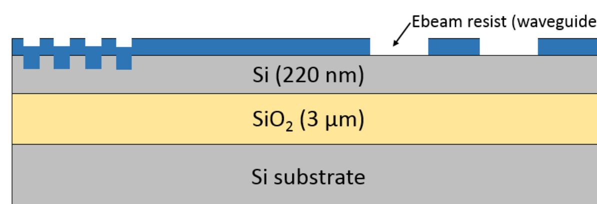
3. Shallow Si ICP etch (70 nm etch depth)



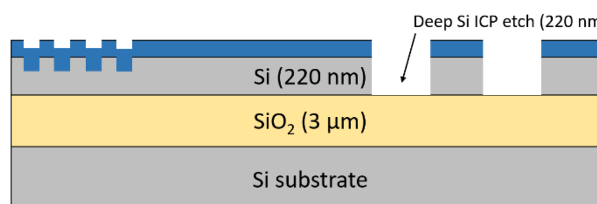
4. E-beam resist strip



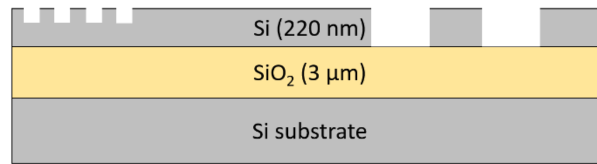
5. E-beam patterning for Silicon Etch 2 (GDS layers 3 & 4) – 220 nm etch



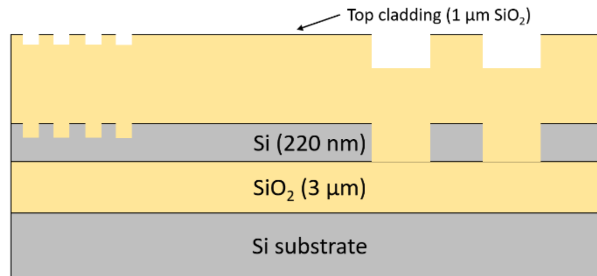
6. Deep Si ICP etch (220 nm etch depth)



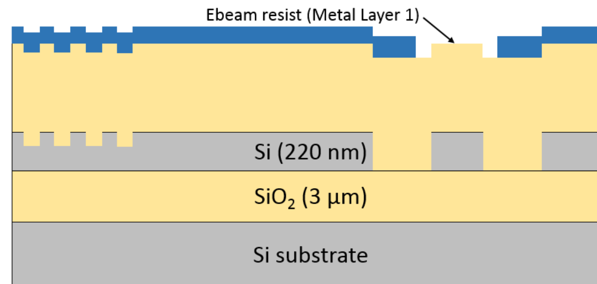
7. E-beam resist strip



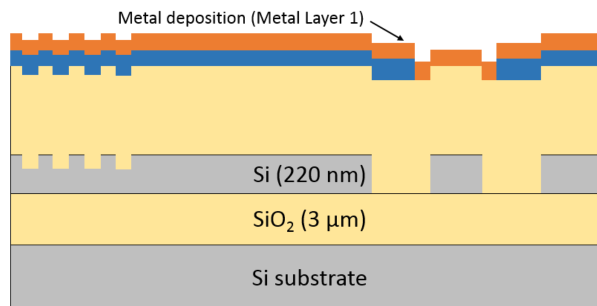
8. Deposition of 1 µm thick silicon dioxide top cladding



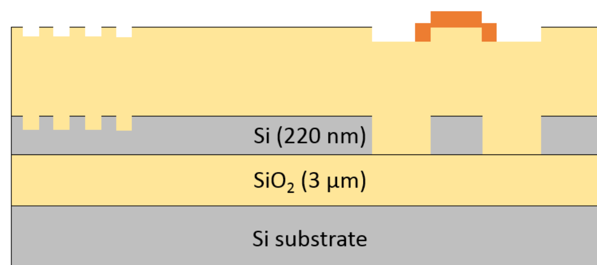
9. E-beam patterning for Metal Layer 1 (GDS layer 39)



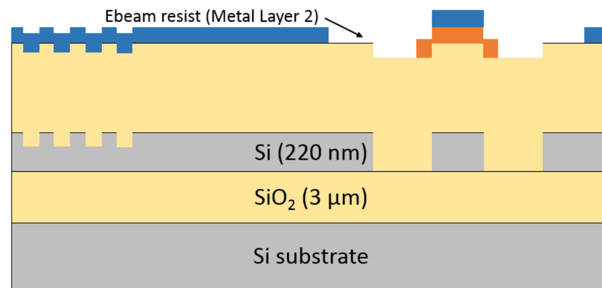
10. Deposition of NiCr for heater filament



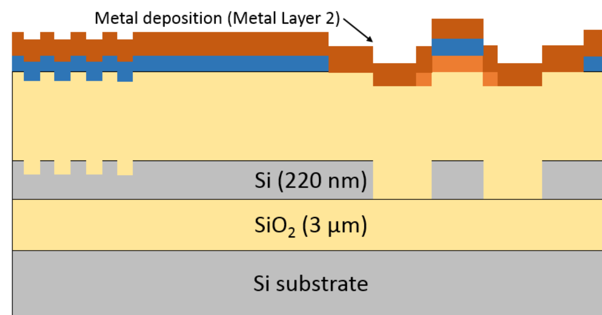
11. Metal lift-off



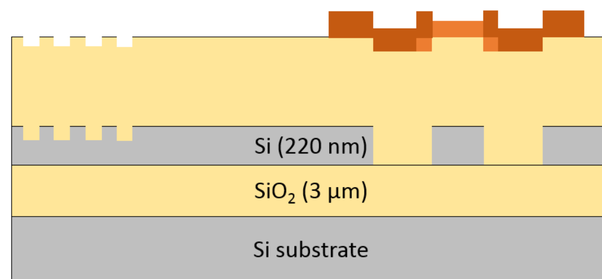
12. E-beam patterning for Metal Layer 2 (GDS layer 13)



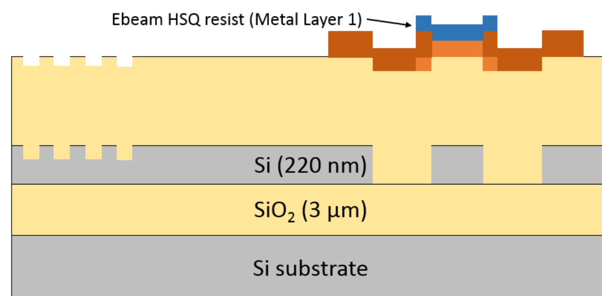
13. Deposition of metal for Ti-Au contact pads and labels



14. Metal lift-off



15. E-beam patterning of HSQ as cladding on heater filament (GDS layer 39)



4. Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (these are not part of the user cell). The test structures that will be checked after fabrication are reported in Table 2 below, together with the optical values that are guaranteed by the CORNERSTONE platform.

Table 2 – Quality assessment parameters.

Test structure	Parameter	Value
Straight waveguides	Propagation loss	< 4 dB/cm for TE mode

5. Mask submission procedure

Ensure that the top cell in your GDSII file is titled 'Cell0_*[Name of Institution]*'.

A website is under construction for GDSII file submission/uploading on or before Friday 30th June 2017. Further details will be circulated nearer the submission deadline. As an alternative, GDSII files can be emailed directly to cornerstone@soton.ac.uk. Ensure that a delivery address, along with contact details (email address & phone number) of the designer are included with all mask submissions.

6. Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE coordinator Dr Callum Littlejohns (cornerstone@soton.ac.uk) or Dr Graham Sharp (graham.sharp@glasgow.ac.uk).

Several standard components such as single mode waveguides, waveguide bends, grating couplers, multi-mode interferometers, ring resonators and Mach-Zehnder interferometers have already been designed and assessed by the CORNERSTONE consortium. Please contact cornerstone@soton.ac.uk should you require the GDSII files or more information on specific components.

7. Device delivery

A total of 4 cells will be delivered to each user. A tentative delivery date of Friday 29th September 2017 has been set.

8. Feedback

Any feedback is always welcomed, including device performance data, future interests for the CORNERSTONE project etc. Email cornerstone@soton.ac.uk with your comments.