CORNERSTONE

Design guidelines for the fourth fabrication call – September 2017

Mask submission deadline – Friday 1st December 2017

1 File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of 1 nm is used, as per the 'CORNERSTONE MPW Run 4 GDSII Template' file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* file.

2 Process flow

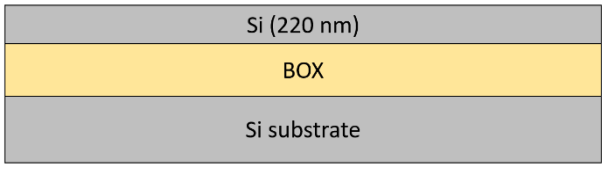
For this fourth call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness $h_{box} > 2$ µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness $h_{wg} = 220$ nm ± 10 nm

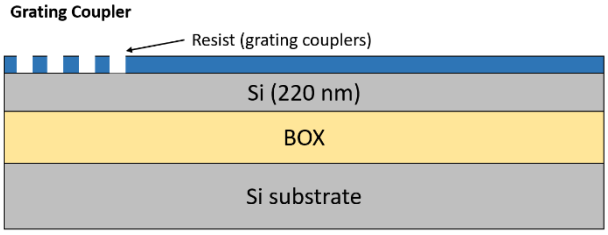
We will offer three silicon etch processes: 1) a shallow silicon etch of 70 nm ± 15 nm, 2) an intermediate silicon etch of 120 nm ± 15 nm, and 3) a continuation silicon etch of a further 100 nm to the BOX layer. We will offer four silicon implantation steps: 1) a low dose *p*-type implant, 2) a low dose *n*-type implant, 3) a high dose *p*-type implant for ohmic contacts, and 4) a high dose *n*-type implant for ohmic contacts. More information on the implant conditions can be found in Section 2.1. We will offer a single metal layer for ohmic silicon contacts, on top of a 1 µm ± 100 nm thick silicon dioxide top cladding layer. In addition, we will offer metal heaters.

The schematic description of the process flow is given below:

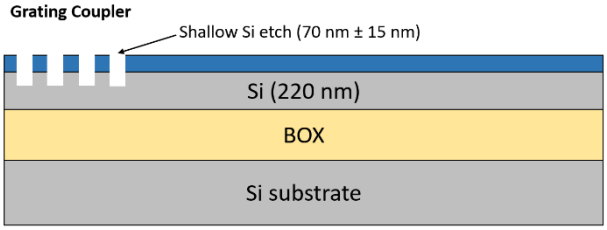
1. Starting SOI substrate



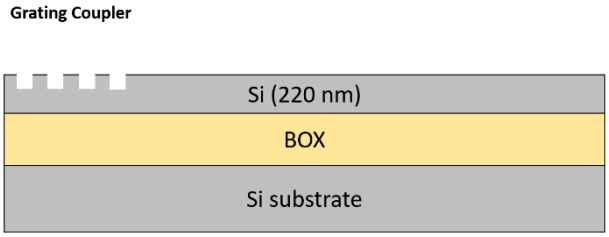
2. Resist patterning for Silicon Etch 1 (GDS layer 6) – 70 nm ± 15 nm etch



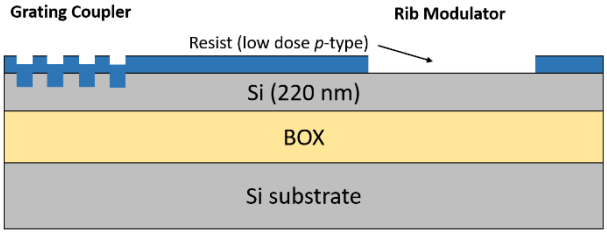
3. Shallow Si etch (70 nm ± 15 nm etch depth)



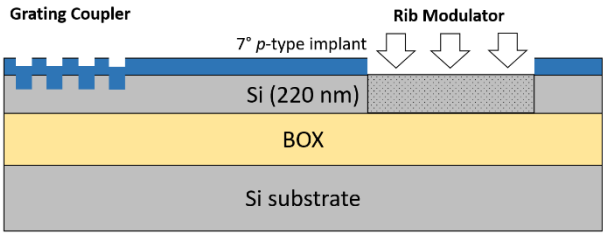
4. Resist strip



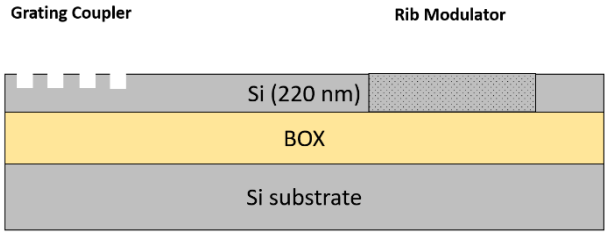
5. Resist patterning for Low Dose *p*-type Implant (GDS layer 7)



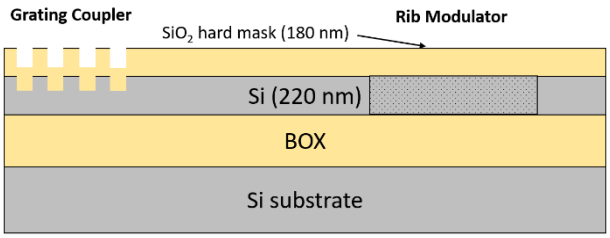
6. Low dose *p*-type implant (7°)



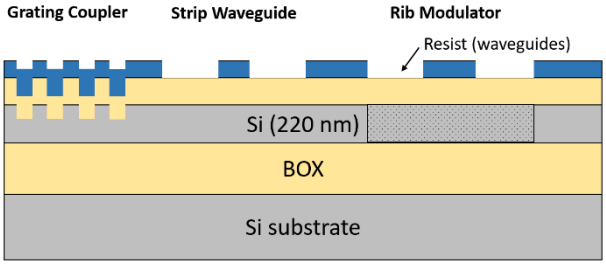
7. Resist strip



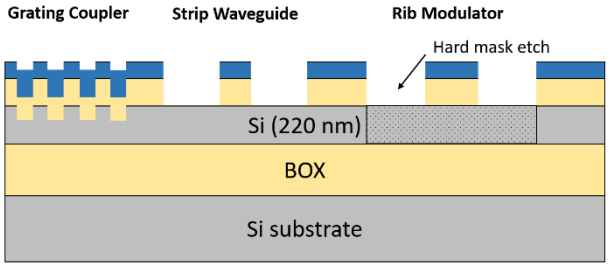
8. Silicon dioxide hard mask deposition – 180 nm



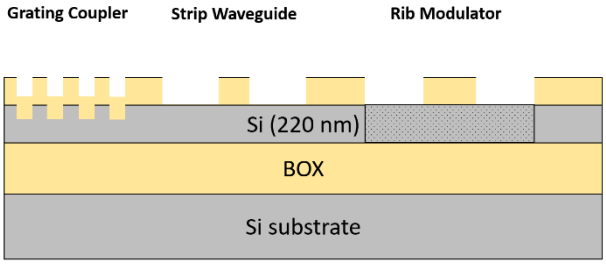
9. Resist patterning for Silicon Etch 2 (GDS layers 3 & 4) – 120 nm ± 15 nm etch



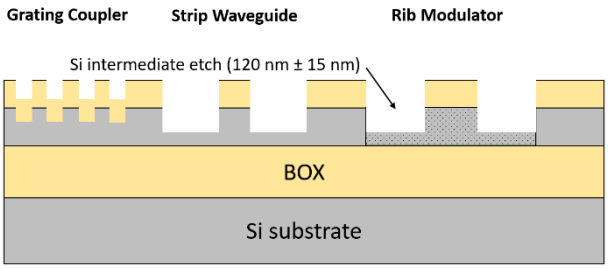
10. Hard mask etch



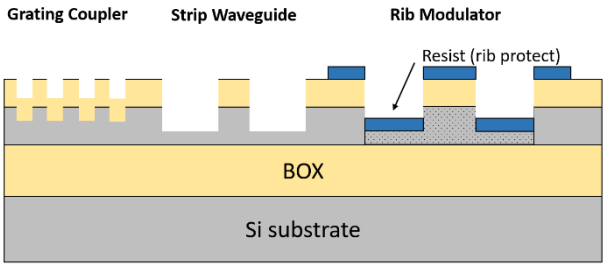
11. Resist strip



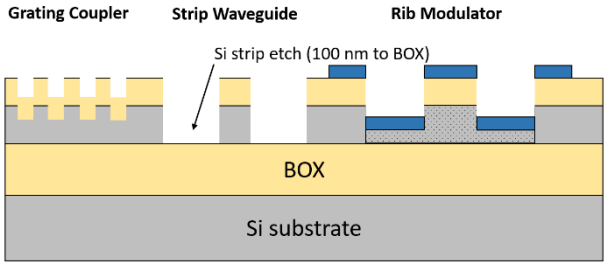
12. Intermediate Si etch (120 nm ± 15 nm etch depth)



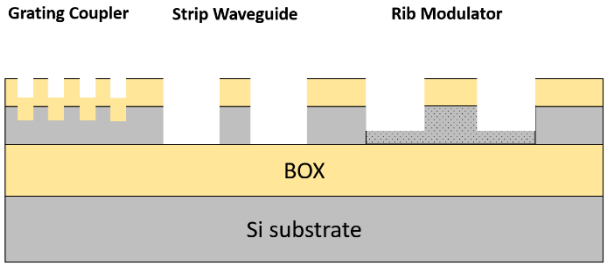
13. Resist patterning for Silicon Etch 3 (GDS layer 5) – 100 nm etch to BOX



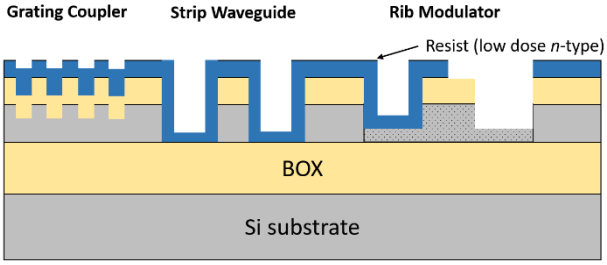
14. Si continuation etch to BOX (100 nm etch to BOX)



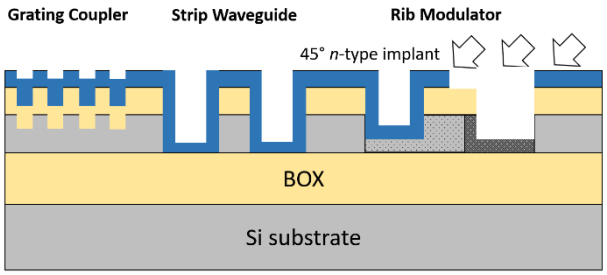
15. Resist strip



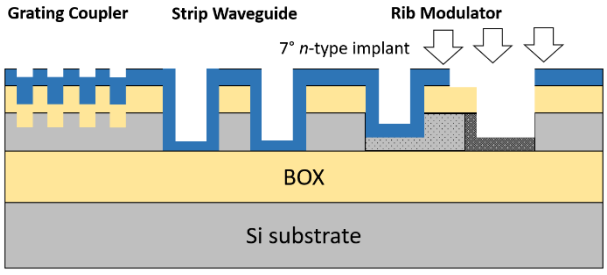
16. Resist patterning for Low Dose *n*-type Implant (GDS layer 8)



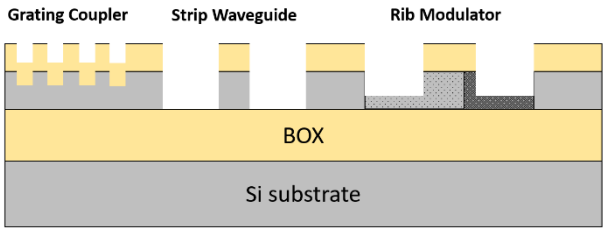
17. Angled low dose *n*-type implant (45°)



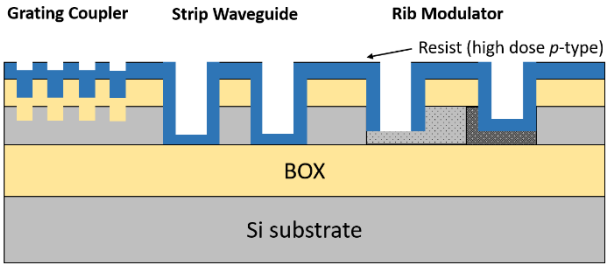
18. Low dose *n*-type implant (7°)



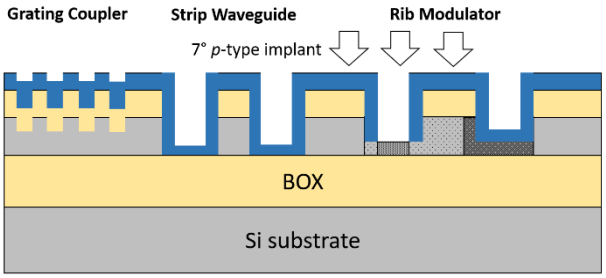
19. Resist strip



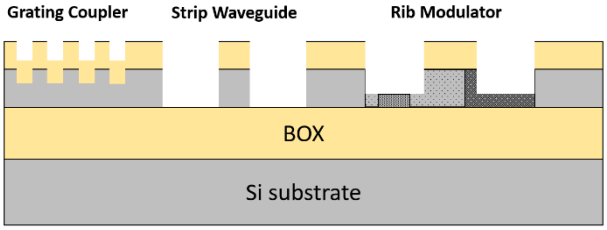
20. Resist patterning for High Dose *p*-type Implant (GDS layer 9)



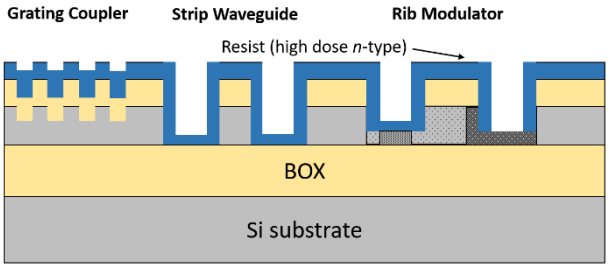
21. High dose *p*-type implant (7°)



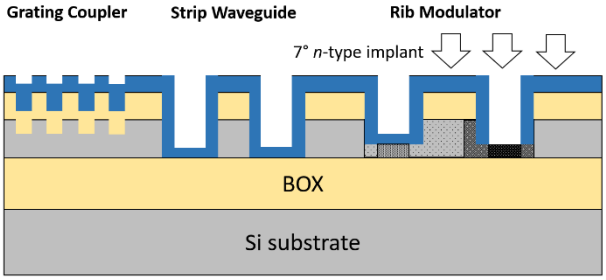
22. Resist strip



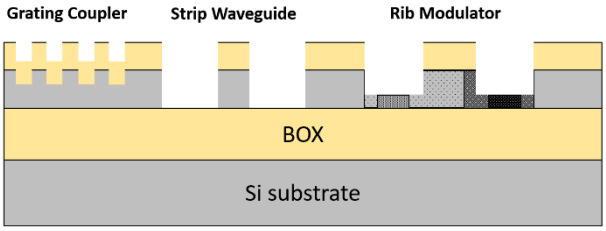
23. Resist patterning for High Dose *n*-type Implant (GDS layer 11)



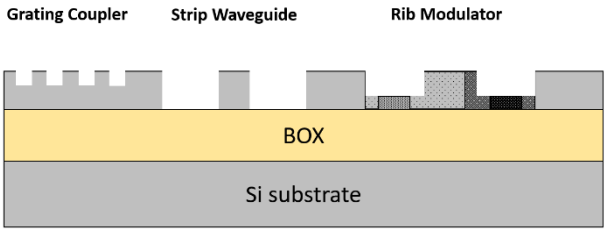
24. High dose *n*-type implant (7°)



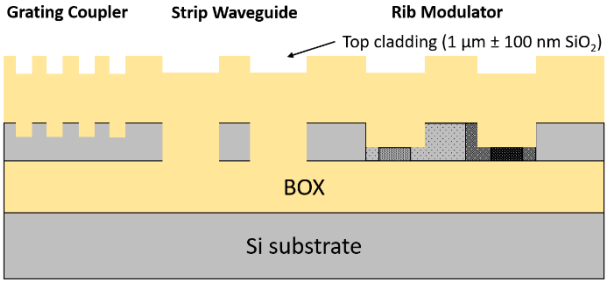
25. Resist strip



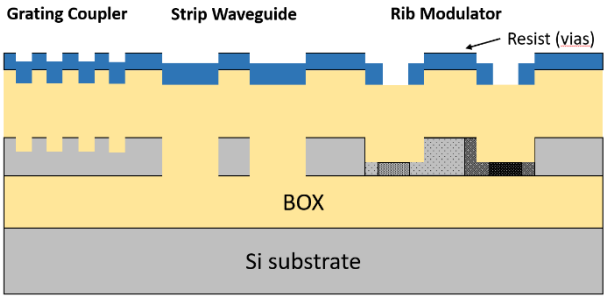
26. Hard mask strip and dopant activation



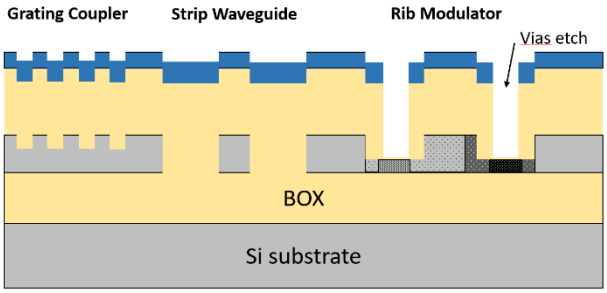
27. Deposition of 1 µm ± 100 nm thick SiO_2 top cladding



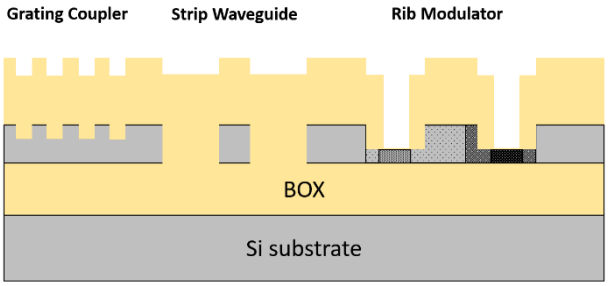
28. Resist patterning for Vias (GDS layer 12)



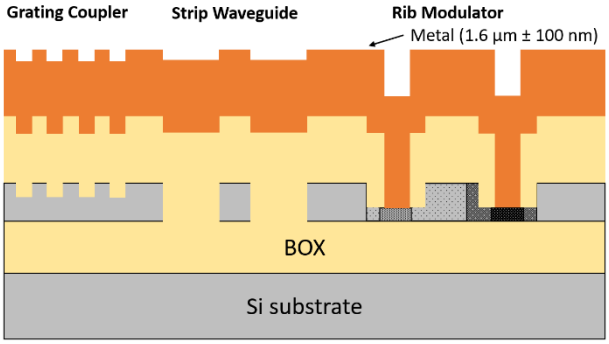
29. SiO_2 vias etch



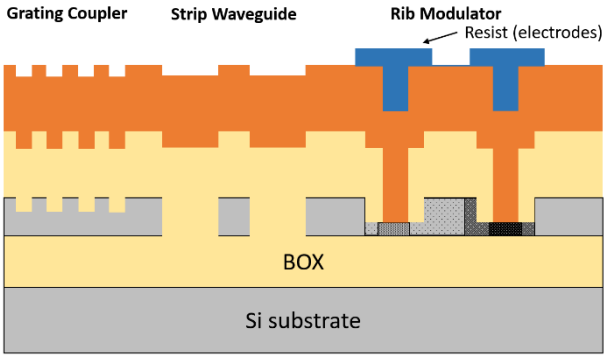
30. Resist strip



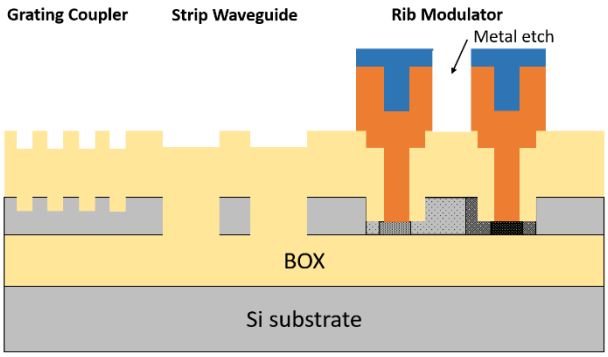
31. Electrode metal stack deposition – 1.6 µm ± 100 nm



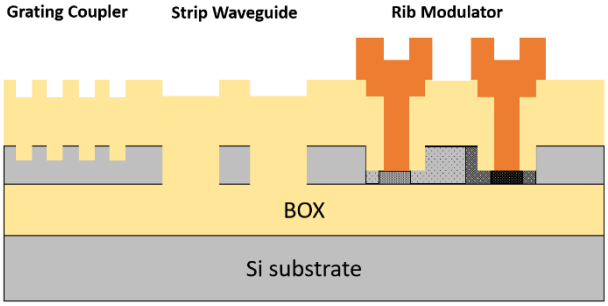
32. Resist patterning for Electrodes (GDS layer 13)



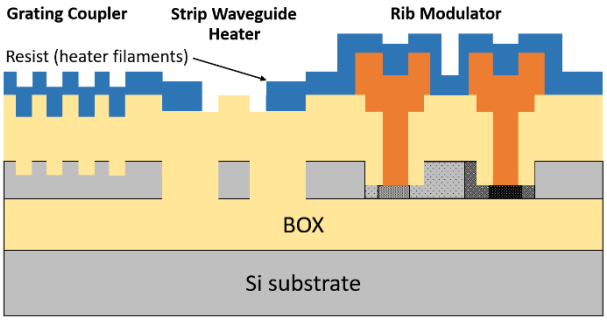
33. Metal etch



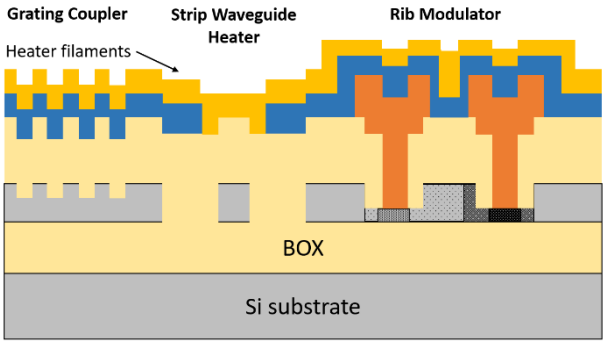
34. Resist strip



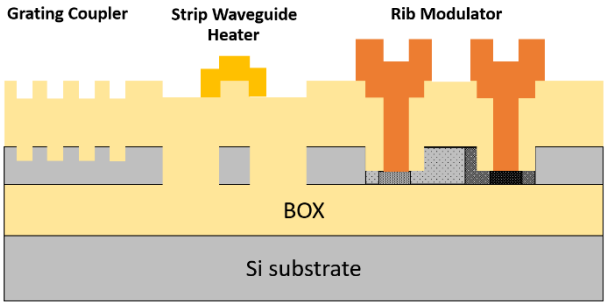
35. Resist patterning for Heater Filaments (GDS layer 39)



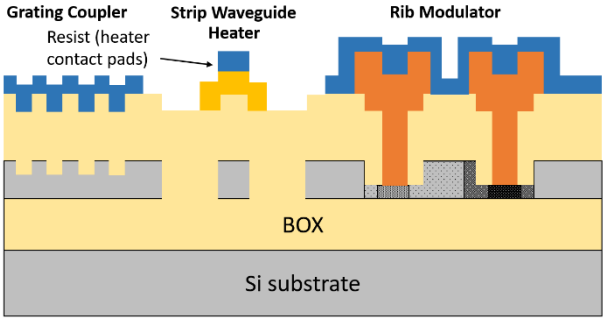
36. Heater filament deposition



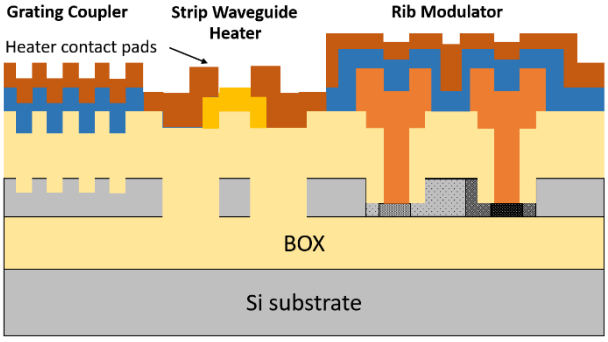
37. Metal lift-off



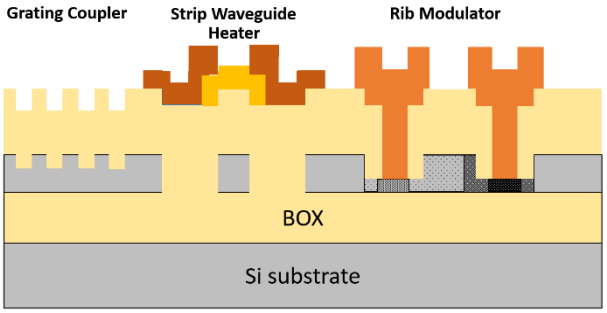
38. Resist patterning for Heater Contact Pads (GDS layer 41)



39. Heater contact pads deposition



40. Metal lift-off



2.1 Process parameters overview

A cross-section of a carrier depletion modulator structure is shown in Figure 1, along with the important device parameters, including doping concentrations, listed in Table 1.

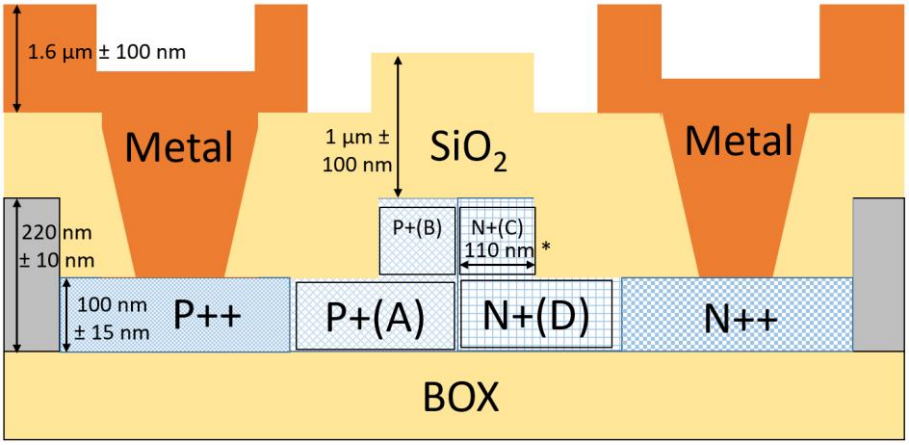


*Figure 1 – Process parameters overview. *The N+ implant is performed at 45°, so the implanted region is fixed at 110 nm from waveguide edge (controlled by the angled implant energy).*

Table 1 – Important device parameters.

Property	Specification
Si overlayer thickness	220 nm ± 10 nm
Grating etch depth	70 nm ± 15 nm
Rib w/g etch depth	120 nm ± 15 nm
P+ region (A)	~3.8E17 cm^{-3}
P+ region (B)	~1.5E17 cm^{-3}
N+ region (C)*	~7.5E17 cm^{-3}
N+ region (D)*	~1.1E18 cm^{-3}
P++	~1E20 cm^{-3}
N++	~1E20 cm^{-3}
Top cladding SiO_2 thickness	1 µm ± 100 nm
Metal thickness	1.6 µm ± 100 nm

**Note:* The low dose *n*-type implant concentrations are compensated by the background low dose *p*-type implant (i.e. the low dose *n*-type region must fully overlap with the low dose p-type region; otherwise, the actual *n*-type concentrations will be higher than specified).

If alternative implant conditions are required, we may be able to perform them for a small charge. Email cornerstone@soton.ac.uk with your request.

3 Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing.

3.1 Design area

The standard user cell has dimensions of **11.47 x 4.9 mm²**. If cleaved facets are required for edge coupling, the total writing area should be reduced to **10.47 x 4.9 mm²** as an overlay (or bleed) of 500 µm should be included on the east and west facets, as shown in Figure 2. Please note that the input/output waveguides should extend fully into the bleed area. If you would like your chips to be cleaved, please indicate this on the submission form when submitting your mask design.

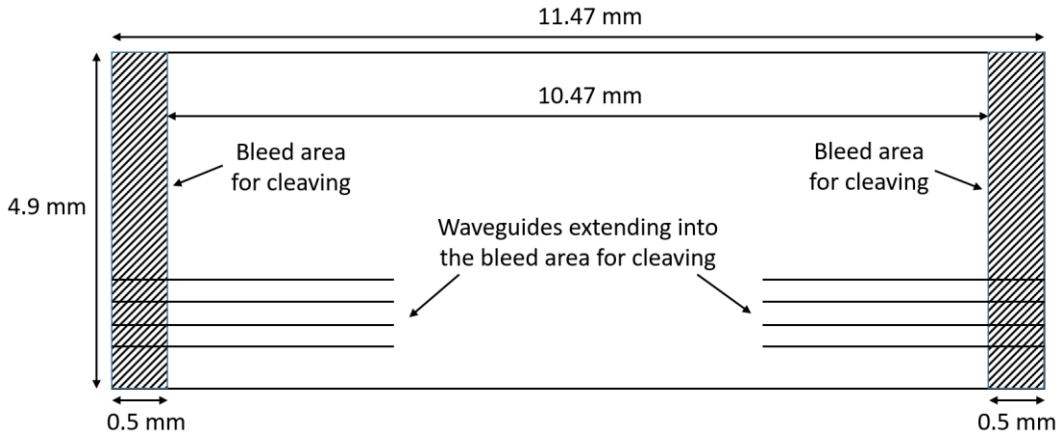


Figure 2 – User cell design area layout.

3.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers) – GDS Layer 6 (Dark field) – etch depth: 70 nm ± 15 nm

This layer is used to define grating couplers, which are fabricated with 70 nm shallow silicon etching. The drawn area is etched.

Silicon Etch 2 (Waveguide layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 15 nm

This layer defines both strip and rib waveguides (to form a rib waveguide, the slab region is protected during Silicon Etch 3, defined by GDS layer 5 – see below), and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching (to the rib waveguide height). During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 3).

GDS Layer 4: Drawn objects on this layer will be exposed to the 120 nm silicon etch (to the rib waveguide height). The pattern density for this layer should be less than 0.5% of the total design area. An example photonic crystal structure is shown in Figure 4. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

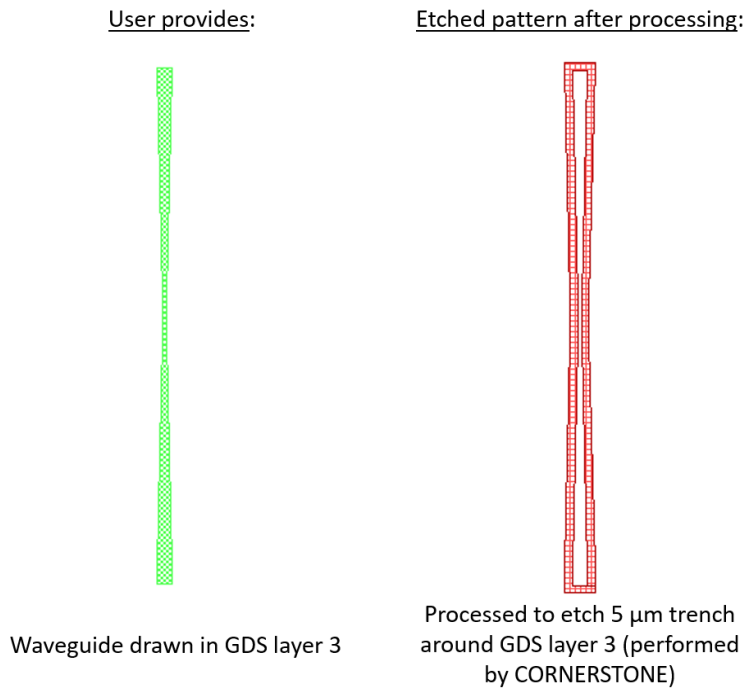


Figure 3 - Description of GDS Layer 3 processing.

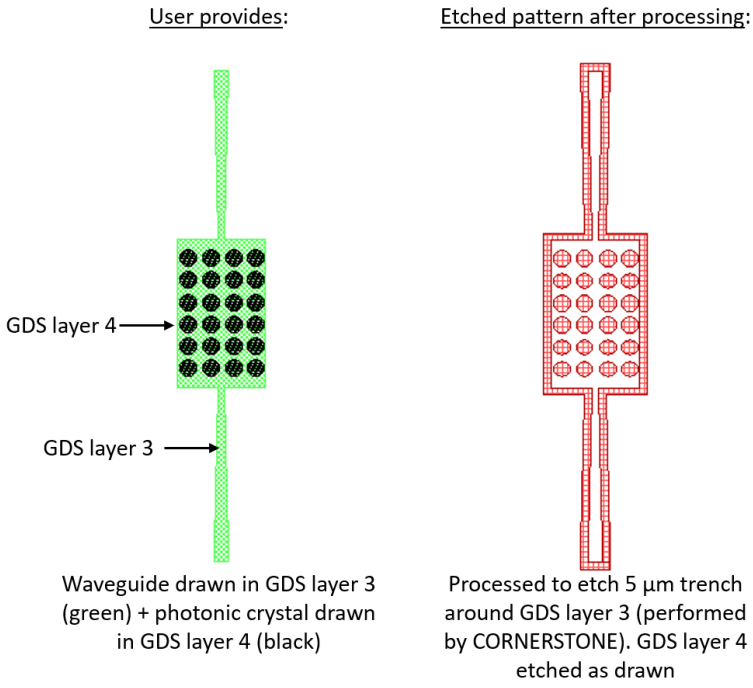


Figure 4 – Example photonic crystal structure using GDS Layers 3 & 4.

Silicon Etch 3 (Rib protect layer) – GDS Layer 5 (Light field) – etch depth: 100 nm to BOX

This layer defines the protective layer for rib waveguides. Drawn objects in this layer will be protected from etching whilst the strip waveguides are etched to the BOX (all areas not previously defined in the Silicon Etch 2 layer will be protected from etching by a hard mask). This layer should extend 10 µm from the waveguide edge, with the exception of any rib-to-strip transitions. An overview of how to draw both strip and rib waveguides is shown in Figure 5.

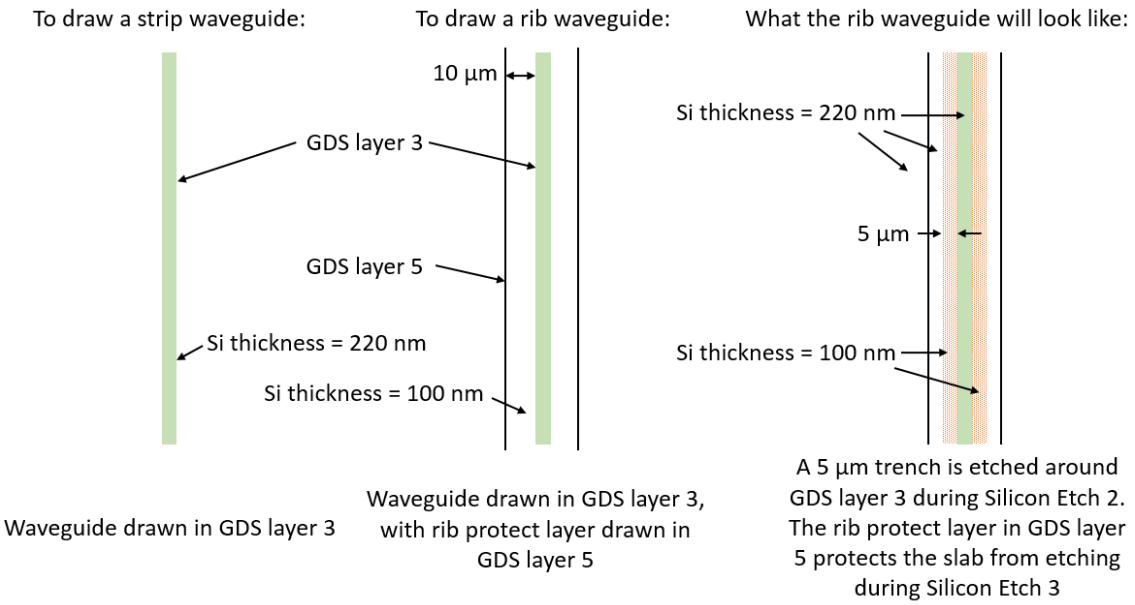


Figure 5 – Drawing strip and rib waveguides.

Low dose p-type Implant – GDS Layer 7 (Dark field)

This layer defines the background low dose *p*-type implant. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 1 in Section 2.1 above.

Low dose n-type Implant – GDS Layer 8 (Dark field)

This layer defines the background low dose *n*-type implant. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 1 in Section 2.1 above. In order for the listed doping concentrations to be valid, the low dose *n*-type region must fully overlap with the low dose *p*-type region. Otherwise, the actual *n*-type concentrations will be higher than specified.

A self-aligned process is used for the low dose *n*-type implant (i.e. the waveguides are etched through an oxide hard mask, and the low dose *n*-type implant is performed with hard mask still in place). Therefore, no matter where the low dose *n*-type edge is drawn within the waveguide, it will be masked from above the waveguide by the hard mask. The implant depth into the waveguide sidewall (45° angled implant) is approximately 110 nm, and is controlled by the implant energy. Therefore, it is best to position the low dose *n*-type implant boundary in the centre of the waveguide to remove any alignment error.

Due to the nature of the 45° angled implant, it is essential that waveguides are orientated correctly if the sidewall is to be implanted. Waveguides to be implanted must propagate in the east to west direction, with only the south sidewall being implanted, as shown in Figure 6. If ring resonator type modulators are desired, it is recommended to use racetrack designs to overcome this limitation.

Note: It is important to consider the shadowing effect of the approximately 700 nm thick resist and 180 nm thick hard mask when drawing the low dose *n*-type implant layer.

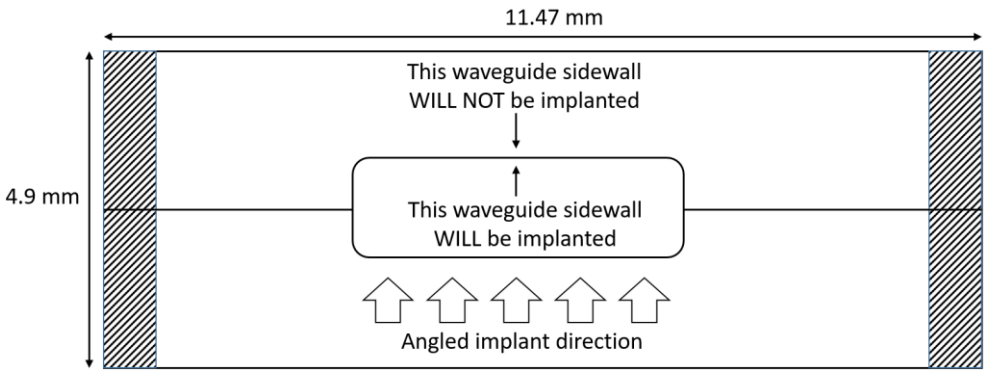


Figure 6 – Orientation of 45° angled n-type implant.

High dose p-type Implant – GDS Layer 9 (Dark field)

This layer defines the high dose *p*-type implant for ohmic Si contacts. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 1 in Section 2.1 above. Implants in this layer will be into the slab region of the waveguide (100 nm Si thickness) i.e. this layer will be merged with the Silicon Etch 2 (Waveguides) and Silicon Etch 3 (Rib protect) layers by CORNERSTONE, as shown in Figure 7.

High dose n-type Implant – GDS Layer 11 (Dark field)

This layer defines the high dose *n*-type implant for ohmic Si contacts. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 1 in Section 2.1 above. Implants in this layer will be into the slab region of the waveguide (100 nm Si thickness) i.e. this layer will be merged with the Silicon Etch 2 (Waveguides) and Silicon Etch 3 (Rib protect) layers by CORNERSTONE, as shown in Figure 7.

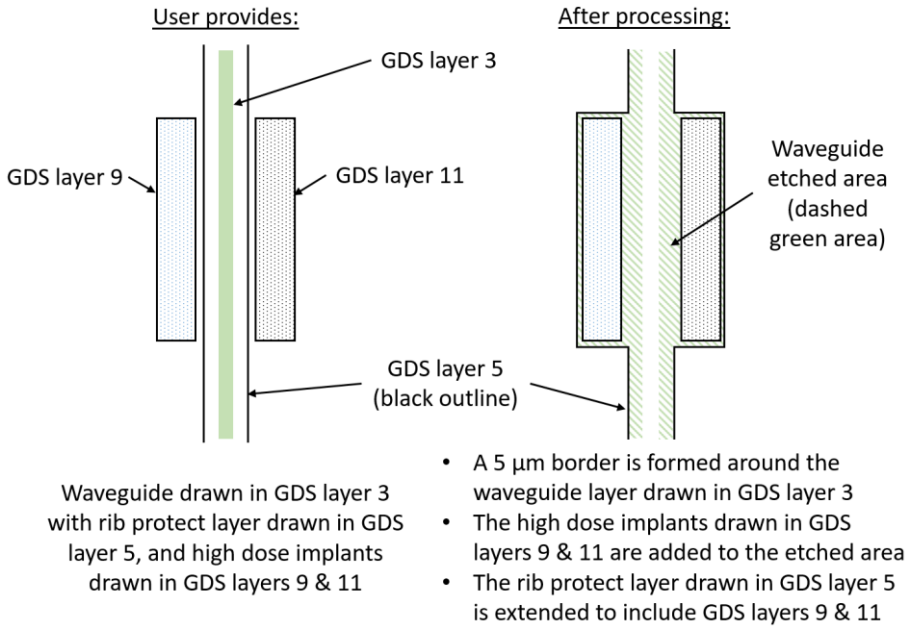


Figure 7 – Processing of high dose implant areas.

Vias – GDS Layer 12 (Dark field)

This layer defines the vias in the 1 µm thick SiO_2 top cladding layer for ohmic Si contacts. Drawn objects in this layer will be etched. All features in this layer must have their corners rounded with a minimum bend radius of 1 µm and recommended bend radius of 2.5 µm, as shown in Figure 8.

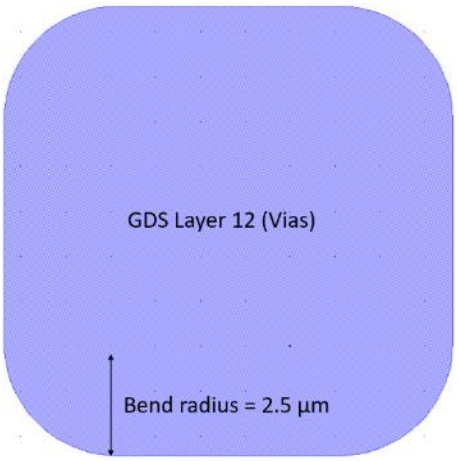


Figure 8 – Rounded features in GDS layer 12 (Vias).

Electrodes – GDS Layer 13 (Light field)

This layer defines the metal electrodes. Drawn objects on this layer will remain after metal etching. The minimum gap between objects drawn in this layer is 2 µm.

Heater Filaments – GDS Layer 39 (Light field)

This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 900 nm for the best compromise between power efficiency and tunability.

Heater Contact Pads – GDS Layer 41 (Light field)

This layer defines the heater contact pads and labels. Drawn objects on this layer will remain after metal lift-off.

An example heater layout for a straight waveguide is included in the *.gdsII* template file. The contact pads can be modified according to your probe design.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2).

Bleed Area – GDS Layer 98

This layer defines the bleed area that will be cleaved if requested by the user. Ensure that waveguides that require cleaving extend fully into this area.

If no cleaving is required, users can fill the entire design space defined in GDS layer 99.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, and will be placed outside the design area.

3.3 Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes, maximum feature widths (where applicable), and maximum pattern densities (where applicable) for each GDS layer are detailed in Table 2.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- All structures drawn in GDS layer 5 (Rib protect) should extend 10 µm beyond the edge of GDS layer 3 (Waveguides), with the exception of rib-to-strip transitions.
- All structures drawn in GDS layer 12 (Vias) must have the corners rounded with a minimum bend radius of 1 µm (recommended bend radius = 2.5 µm).
- All structures drawn in GDS layer 12 (Vias) must be inclusive of either GDS layer 9 (High Dose *p*-type Implant) or GDS layer 11 (High Dose *n*-type Implant) by at least 500 nm (i.e. the high dose implant layer must extend in all directions at least 500 nm beyond the vias layer).
- All structures drawn in GDS layer 12 (Vias) must be inclusive of the metal contacts drawn in GDS layer 13 (Electrodes) by at least 500 nm (i.e. the electrode layer must extend in all directions at least 500 nm beyond the vias layer).
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 12 (Vias) or any of the metal/heater layers.

3.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 2 below.

Table 2 – Design rules summary.

Layer description	GDS number	Field	Max. pattern density	Min. feature size	Max. feature width
Silicon Etch 1 (70 nm ± 15 nm)	6	Dark	N/a	250 nm	N/a
Silicon Etch 2 (120 nm ± 15 nm)	3	Light	N/a	250 nm	N/a
	4	Dark	0.5%		
Silicon Etch 3 (100 nm to BOX)	5	Light	N/a	250 nm	N/a
Low Dose *p*-type Implant	7	Dark	N/a	250 nm	40 µm
Low Dose *n*-type Implant	8	Dark	N/a	250 nm	10 µm
High Dose *p*-type Implant	9	Dark	N/a	250 nm	10 µm
High Dose *n*-type Implant	11	Dark	N/a	250 nm	10 µm
Vias (rounded feature corners)	12	Dark	N/a	3 µm	10 µm
Electrodes*	13	Light	25%	6 µm	N/a
Heater Filaments	39	Light	N/a	900 nm	1.4 µm
Heater Contact Pads	41	Light	10%	2 µm	N/a
Cell Outline	99	N/a	N/a	N/a	N/a
Bleed Area	98	N/a	N/a	N/a	N/a

*Minimum gap between features in electrode layer = 2 µm.

3.5 GDSII template file

A *.gdsII* template file titled 'CORNERSTONE MPW Run 4 GDSII Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

4 Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the optical values that are guaranteed by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight rib waveguide	Propagation loss	< 4 dB/cm for TE mode
1.8 mm long MZI based carrier depletion modulator	Speed @ 2 V dual drive	28 Gb/s
	Insertion loss @ 2 V dual drive	< 5 dB
	Extinction ratio @ 2 V dual drive	> 3 dB

5 Mask submission procedure

Ensure that the top cell in your .gdsII file is titled 'Cell0_*[Name of Institution]*'.

In order to submit your mask design on or before **Friday 1st December 2017**, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/mask-submission

After completion and submission of the form, within 24 hours you will be emailed a link to the mask uploading module, along with a username and password to sign in. Upload your *.gdsII* file to the CORNERSTONE MPW Run 4 folder, from where the CORNERSTONE team will be able to access it.

Note: Other CORNERSTONE users will not be able to view your uploaded files.

6 Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE co-ordinator Dr Callum Littlejohns (cornerstone@soton.ac.uk) or Dr Graham Sharp (graham.sharp@glasgow.ac.uk).

Several standard components such as single mode waveguides, waveguide bends, grating couplers, multi-mode interferometers (MMI's), angled MMI's for wavelength division multiplexing, ring resonators, Mach-Zehnder interferometers (MZI's), carrier depletion MZI modulators, and heaters have already been designed and assessed by the CORNERSTONE team. Please contact cornerstone@soton.ac.uk should you require the *.gdsII* files or more information on specific components.

7 Device delivery

A total of 3 replica cells will be delivered to each user. A tentative delivery date of Friday 27th July 2018 has been set.

8 Feedback

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the customer satisfaction, and a measure to what extent we were able to meet customer requirements. Therefore, we kindly ask our customers to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips. Alternatively, email cornerstone@soton.ac.uk with your comments.

9 Publication

If you are submitting designs as a UK research institution and have access to the CORNERSTONE platform free of charge, then please contact cornerstone@soton.ac.uk for a list of authors to include on any publications. Otherwise, please include CORNERSTONE in the acknowledgments section of any publications.